AMENDMENTS TO CLAIMS

- Please delete claims 11, 12, 16, and 17.
- Please amend pending claims 5 and 9 as indicated below. A complete listing of all claims and their status in the application are as follows:

1. (previously presented) A method of manufacturing a heterojunction bipolar transistor comprising:

providing a semiconductor substrate having a collector region;

forming an intrinsic base region of a compound semiconductive material over the collector region;

forming a reverse emitter window over a portion of the intrinsic base region;

forming a polysilicon layer over the reverse emitter window and the remaining portion of the intrinsic base region;

performing a chemical mechanical polish of the polysilicon layer to level the upper surface of the polysilicon layer with the upper surface of the reverse emitter window;

recessing the polysilicon layer below the upper surface of the reverse emitter window to form an extrinsic base structure over a remaining portion of the intrinsic base region;

growing a dielectric layer over the extrinsic base structure;

processing the reverse emitter window to form an emitter window having a multi-layer reverse insulating spacer therein;

forming an emitter structure in the emitter window;

forming an interlevel dielectric layer over the collector region, extrinsic base structure and emitter structure; and

forming connections through the interlevel dielectric layer to the collector region, the extrinsic base structure, and the emitter structure.

2. (original) The method as claimed in claim 1 wherein forming the intrinsic base region comprises forming a layer of compound semiconductive material of silicon-germanium, silicon-germanium-carbon, or a combination thereof.

3. (original) The method as claimed in claim 1 wherein forming the intrinsic base region comprises forming a compound semiconductive material layer by selectively depositing, selectively growing, or field depositing, or a combination thereof.

4. (previously presented) The method as claimed in claim 1 wherein:

forming the reverse emitter window comprises forming a first insulating layer and a second insulating layer; and

processing the reverse emitter window comprises anisotropically etching the first insulating layer and the second insulating layer to form an emitter window having a multi-layer reverse insulating spacer therein.

5. (currently amended) The method as claimed in claim 1 wherein_forming an intrinsic base region of a compound semiconductive material over the collector region forms the intrinsic base region in the bottom and on the sides of the emitter window.

6. (previously presented) A method of manufacturing a heterojunction bipolar transistor comprising:

providing a semiconductor substrate having a collector region;

forming an intrinsic base region of a compound semiconductive material over the collector region;

forming a reverse emitter window over the intrinsic base region;

forming a first polysilicon layer over a portion of the intrinsic base region uncovered by the reverse emitter window;

performing a chemical mechanical polish of the polysilicon layer to level the upper surface of the polysilicon layer with the upper surface of the reverse emitter window;

recessing the polysilicon layer below the upper surface of the reverse emitter window to form an extrinsic base structure over the intrinsic base region uncovered by the reverse emitter window;

growing a dielectric layer over the first polysilicon layer;

processing the reverse emitter window to form an emitter window having a multi-layer reverse insulating spacer therein;

forming a second polysilicon layer over the dielectric layer and into the emitter window;

processing the second polysilicon layer to form an emitter structure;

processing the first polysilicon layer to form an extrinsic base structure over a portion of the intrinsic base region beside and spaced from the emitter structure;

forming an interlevel dielectric layer over the collector region, the extrinsic base structure, and the emitter structure; and

forming connections through the interlayer dielectric layer to the collector region, the extrinsic base structure, and the emitter structure.

7. (original) The method as claimed in claim 6 wherein forming the intrinsic base region comprises forming a layer of compound semiconductive material of silicon-germanium, silicon-germanium-carbon, or a combination thereof.

8. (original) The method as claimed in claim 6 wherein forming the intrinsic base region comprises forming a compound semiconductive material layer by selectively depositing, selectively growing, or field depositing, or a combination thereof.

9. (currently amended) The method as claimed in claim 6 wherein:

forming the reverse emitter window comprises forming a first insulating layer and a second insulating layer; and

processing the reverse emitter window comprises anisotropically etching the first insulating layer and the second insulating layer to form an emitter window having a multi-layer reverse insulating spacer therein.

10. (currently amended) The method as claimed in claim 6 wherein forming an intrinsic base region of a compound semiconductive material over the collector region forms the intrinsic base region in the bottom and on the sides of the emitter window.

11. (cancelled)

12. (cancelled)

13. (cancelled)

14. (cancelled)

15. (cancelled)

16. (cancelled)

17. (cancelled

18. (cancelled)

19. (cancelled)

20. (cancelled)